LESSON PLAN FOR Digital Electronics & Microprocessor (Th3)		
Discipline: Electrical Engineering	**Semester:** 5th	**Name of the Teaching Faculty:** Ms. Deepika sarkar (Lect. In ETC)
Subject: Digital Electronics & Microprocessor	**No. of days per week class allotted:** 5	**Semester start From Date :** 15.09.2022 **to Date :** 22.12.2022 **No. of Weeks:** 13 **Session:** 2022-23
Week	**Class Day**	**Theory**
1st		**1. BASICS OF DIGITAL ELECTRONICS**
	1st	Introduction to course content
	2nd	1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	3rd	1.2 Binary addition, subtraction, Multiplication and Division.
	4th	1.3 1's complement and 2's complement numbers for a binary number .
	5th	1.4 Subtraction of binary numbers in 2's complement method.
2nd	1st	1.5 Use of weighted and Un-weighted codes & write Binary equivalent number & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa (contd.).1.6 Importance of parity Bit.
	2nd	1.5 Use of weighted and Un-weighted codes & write Binary equivalent number & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.
	3rd	1.6 Importance of parity Bit.
	4th	1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	5th	1.8 Realize AND, OR, NOT operations using NAND, NOR gates.
3rd	1st	1.9 Different postulates and De-Morgan's theorems in Boolean algebra
	2nd	1.10 Use Of Boolean Algebra For Simplification Of Logic Expression.
	3rd	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.(contd.)
	4th	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.(contd.)
	5th	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
4th		**2. COMBINATIONAL LOGIC CIRCUITS**
	1st	2.1 Give the concept of combinational logic circuits.
	2nd	2.2 Half adder circuit and verify its functionality using truth table.
	3rd	2.3 Realize a Half-adder using NAND gates only and NOR gates only.
	4th	2.4 Full adder circuit and explain its operation with truth table.
	5th	2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table
5th	1st	2.6 Full subtractor circuit.and explain its operation with truth table.

5th	2nd	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer.
	3rd	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	4th	2.9 Working of Two bit magnitude comparator.
	5th	Question answer session.
		3. SEQUENTIAL LOGIC CIRCUITS
	1st	3.1 Give the idea of Sequential logic circuits.
	2nd	3.2 State the necessity of clock and give the concept of level clocking and edge triggering,
	3rd	3.3 Clocked SR flip flop with preset and clear inputs.
	4th	3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
6th	5th	3.6 Concept of race around condition and study of master slave JK flip flop.
7th	1st	3.7 Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	2nd	3.8 Applications of flip flops.
	3rd	3.9 Define modulus of a counter
	4th	3.10 4-bit asynchronous counter and its timing diagram.
	5th	3.11 Asynchronous decade counter.
	1st	3.12 4-bit synchronous counter.
	2nd	3.13 Distinguish between synchronous and asynchronous counters.
	3rd	3.14 State the need for a Register and list the four types of registers.
	4th	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.
8th	5th	Question answer session.
		4. 8085 MICROPROCESSOR
	1st	4.1 Introduction to Microprocessors, Microcomputers
	2nd	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	3rd	4.3 Pin diagram and description.
	4th	4.4 Stack, Stack pointer & stack top
9th	5th	4.5 Interrupts
10th	1st	4.6 Opcode & Operand,
	2nd	4.7 Differentiate between one byte two byte & three byte instruction with example.
	3rd	4.8 Instruction set of 8085 example
	4th	4.9 Addressing mode(cont.)
	5th	4.9 Addressing mode
	1st	4 .10 Fetch Cycle, (cont.)
	2nd	Machine Cycle, Instruction Cycle, T-State.
	3rd	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write.
	4th	4.12 Timing Diagram for 8085 instruction
11th	5th	4.13 Counter and time delay.
12th	1st	4. 14 Simple assembly language programming of 8085.(contd.)

12th	2nd	4. 14 Simple assembly language programming of 8085.
		5. INTERFACING AND SUPPORT CHIPS
	3rd	5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping.
	4th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 (cont)
	5th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 .
	1st	5.3 Application using 8255:
	2nd	Seven segment LED display.
	3rd	Square wave generator.
	4th	Traffic light Controller.
13th	5th	class test-2

14/09/2022

HOD
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14/09/2022

Academic co-ordinator

Principal
Govt. polytechnic Nabarangpur

14/9/22