LESSON PLAN FOR Digital Electronics & Microprocessor (Th3)		
Discipline: Electrical Engineering	**Semester:** 5th	**Name of the Teaching Faculty: Ms. Deepika sarkar (Lect. In ETC)**
Subject: Digital Electronics & Microprocessor	**No. of days per week class allotted: 5**	**Semester From Date : 01.08.2023 to Date: 30.11.2023** **Required No. of Weeks: 15 Session:-2023-34**
Week	**Class Day**	**Theory**
1st		**1. BASICS OF DIGITAL ELECTRONICS**
	1st	Introduction to course content
	2nd	1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	3rd	1.2 Binary addition, subtraction, Multiplication and Division.
	4th	1.3 1's complement and 2's complement numbers for a binary number
	5th	1.4 Subtraction of binary numbers in 2's complement method.
2nd	1st	1.5 Use of weighted and Un-weighted codes & write Binary equivalent number (cont.)
	2nd	& write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.
	3rd	1.6 Importance of parity Bit.
	4th	1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	5th	1.8 Realize AND, OR, NOT operations using NAND, NOR gates.
3rd	1st	1.9 Different postulates and De-Morgan's theorems in Boolean algebra.
	2nd	1.10 Use Of Boolean Algebra For Simplification Of Logic Expression
	3rd	1.11 Karnaugh Map For 2,3,4 Variable, (cont.)
	4th	Simplification Of SOP And POS Logic Expression Using K-Map.
	5th	Doubt clearing session .
4th		**2. COMBINATIONAL LOGIC CIRCUITS**
	1st	2.1 Give the concept of combinational logic circuits.
	2nd	2.2 Half adder circuit and verify its functionality using truth table.
	3rd	2.3 Realize a Half-adder using NAND gates only(cont.)
	4th	and NOR gates only.
	5th	2.4 Full adder circuit and explain its operation with truth table.
5th	1st	2.5 Realize full-adder using two Half-adders and an OR – gate(cont.)
	2nd	and write truth table
	3rd	2.6 Full subtractor circuit.(con.)
	4th	and explain its operation with truth table.

	5th	2.7 Operation of 4 X 1 Multiplexers(cont.)
	1st	and 1 X 4 demultiplexer.
	2nd	2.8 Working of Binary-Decimal Encoder(cont.)
	3rd	& 3 X 8 Decoder.
	4th	2.9 Working of Two bit magnitude comparator.
6th	5th	Unit test
		3. SEQUENTIAL LOGIC CIRCUITS
	1st	3.1 Give the idea of Sequential logic circuits.
7th	2nd	3.2 State the necessity of clock and give the concept of level clocking and edge triggering,
	3rd	3.3 Clocked SR flip flop with preset and clear inputs.
	4th	3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	5th	3.6 Concept of race around condition and study of master slave JK flip flop.
	1st	3.7 Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	2nd	3.8 Applications of flip flops.
	3rd	3.9 Define modulus of a counter
	4th	3.10 4-bit asynchronous counter and its timing diagram.
8th	5th	3.11 Asynchronous decade counter.
	1st	3.12 4-bit synchronous counter.
	2nd	3.13 Distinguish between synchronous and asynchronous counters.
	3rd	3.14 State the need for a Register and list the four types of registers.
	4th	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.
9th	5th	Doubt clearing session.
		4. 8085 MICROPROCESSOR
	1st	4.1 Introduction to Microprocessors, Microcomputers
10th	2nd	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	3rd	4.3 Pin diagram and description.
	4th	4.4 Stack, Stack pointer & stack top
	5th	4.5 Interrupts
	1st	4.6 Opcode & Operand,
	2nd	4.7 Differentiate between one byte(cont.)
	3rd	two byte & three byte instruction with example.
	4th	4.8 Instruction set of 8085 example
11th	5th	4.9 Addressing mode(cont.)
	1st	4.9 Addressing mode
	2nd	4.9 Addressing mode
	3rd	4 .10 Fetch Cycle, (cont.)
	4th	Machine Cycle, Instruction Cycle, T-State.
12th	5th	4.11 Timing Diagram for memory read,
	1st	memory write, I/O read, I/O write.
	2nd	4.12 Timing Diagram for 8085 instruction
13th	3rd	4.13 Counter and time delay.

	4th	4. 14 Simple assembly language programming of 8085.
	5th	Doubt clearing session.
14th		**5. INTERFACING AND SUPPORT CHIPS**
	1st	5.1 Basic Interfacing Concepts, Memory mapping(cont.)
	2nd	& I/O mapping.
	3rd	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 (cont)
	4th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 .(cont.)
	5th	.5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
15th	1st	5.3 Application using 8255:
	2nd	Seven segment LED display.
	3rd	Square wave generator.
	4th	Traffic light Controller.
	5th	Last unit tset

Faculty 31/07/23

HOD 31/07/2023
Electrical Engg.

Academic coordinator 31/07/23

Principal 31/7/23
Govt polytechnic Nabarangpur